IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method comprising:

detecting a condition of an integrated circuit having a test-access port (TAP) [[TAP]] while communicating through a TAP-control selector with the TAP using an automatic tester ~~a first TAP control device~~;

freezing the integrated circuit in a logic state in response to the detected condition;

switching control of the test-access port from the automatic tester to a TAP master controller after freezing the integrated circuit in the logic state; and

communicating through the TAP-control selector with the TAP using the TAP master controller ~~a second TAP control device~~ in response to detecting the condition in order to dump state values from the integrated circuit into a memory of the TAP master controller.

2. (Currently Amended) The method of claim 1, wherein communicating with the TAP using the TAP master controller ~~a second control device~~ occurs ~~in response to detecting the condition and~~ by having the automatic tester issuing a ~~second~~ control signal to the TAP master controller ~~the second control device~~.

3. (Original) The method of claim 1, wherein the condition is a failure of the integrated circuit.

4. (Currently Amended) The method of claim 1:

wherein the condition is associated with a set of state data in the integrated circuit; and

wherein communicating with the TAP using ~~a second~~ the TAP master controller ~~control device,~~ comprises reading the set of state data using the ~~second~~ TAP master controller ~~control device~~.

5. (Currently Amended) The method of claim 1, further comprising:

maintaining the integrated circuit in the detected condition; and

coupling the ~~second~~ TAP master controller ~~control device~~ to the TAP while maintaining the integrated circuit in the detected condition.

6. (Currently Amended) The method of claim 5, wherein coupling the ~~second~~ TAP master controller ~~control device~~ to the TAP occurs in response to asserting a ~~first~~ control signal on a control input of the TAP-control selector ~~from the first TAP control device~~.

7. (Currently Amended) A method comprising:

inputting test data from a ~~first~~ pattern memory ~~device~~ through a TAP-control selector and then to a test-access port of an integrated circuit; and

dumping the desired logic state data and storing the desired logic state data associated with the input test data and output through the TAP-control selector from the test-access port ~~in a second device have~~ into a memory of a TAP master controller, wherein the memory of the TAP master controller has a lower nominal speed rating than the ~~first~~ pattern memory ~~device~~, wherein storing the desired logic state data associated with the input test data occurs after:

detecting existence of a desired condition of the integrated circuit; ~~and~~

decoupling the ~~first~~ pattern memory ~~device~~ from at least a portion of the test access port; and

coupling the memory of the TAP master controller to the test-access port of the integrated circuit.

8. (Currently Amended) The method of claim 7, wherein the ~~first~~ pattern memory ~~device~~ stores vector test-pattern data and wherein the ~~second~~ memory ~~device~~ included in the TAP master controller does not store the vector test-pattern data.

9. (Canceled)

10. (Currently Amended) A system comprising:

first means for controlling a test-access port of an integrated circuit;

second means for controlling the test-access port; and

a multiplexer module, coupled between the test-access port and the first means and between the test-access port and the second means, for selectively coupling the first or second means to the test-access port,

wherein the first means for controlling the test-access port includes a pattern memory operable to store test pattern data for testing the integrated circuit, the first means operable to assert a control signal applied to the multiplexer module when a failed condition is detected during testing of the integrated circuit, the control signal operable to cause the multiplexer module to selectively couple the second means to the test access port, and wherein the first and second means are external to the integrated circuit.

11. (Original) The system of claim 10:

wherein the first and second means include respective first and second sets of signal nodes for outputting or receiving signals from a test-access port; and

wherein the multiplexer module includes first and second multiplexers, with each multiplexer having a first input node coupled to one of the signal nodes in the first set of signal nodes and a second input node coupled to one of the signal nodes in the second set of signal nodes.

12. (Original) The system of claim 10, further comprising means for communicating a control signal from the first means to the second means to coordinate control of the test-access port.

13. (Original) The system of claim 10, wherein the first and second sets of signal nodes output or receive respective sets of JTAG signals.

14. (Currently Amended) Apparatus comprising:

a ~~first TAP control device~~ tester having a first node for connection to a ~~test~~ test-access port (TAP) of an integrated circuit; and

a multiplexer including a control input, and including first and second selectable nodes and a non-selectable node, with the first selectable node coupled to the first node of the tester ~~first TAP control device~~, the second selectable node coupled to a TAP master controller, and the non-selectable node ~~for connection~~ coupled to the ~~test~~ test-access port, the control input operable to selectively couple either the first selectable node or the second selectable node to the non-selectable node based on a control signal;

wherein the tester is operable to assert a control signal on the control input of the multiplexer causing the multiplexer to selectably couple the second selectable node to the non-selectable node when a targeted test condition occurs on the integrated circuit, and

wherein the ~~first~~ tester, the TAP master controller, ~~control device~~ and the multiplexer are all external to the integrated circuit.

15. (Currently Amended) The apparatus of claim 14, ~~further comprising a second~~ the TAP master controller including a memory and a boundary scan controller ~~control device having a second node coupled to the second selectable node of the multiplexer~~.

16. (Currently Amended) The apparatus of claim 14, further comprising a ~~vector pattern memory or algorithmic~~ pattern generator included in the tester ~~coupled to the first TAP control device~~.

17. (Currently Amended) The apparatus of claim 14, wherein the first TAP master controller ~~control device~~ comprises a JTAG compliant boundary-scan controller.

18. (Currently Amended) Apparatus for selecting control of a test-access port of an integrated circuit, comprising:

first means for electrical connection to a node of a tester ~~first TAP control device~~;

second means for electrical connection to a node of a ~~second~~ TAP master controller ~~control device~~;

third means for electrical connection to a node of a test-access-port of an integrated circuit; and

a first multiplexer coupled to the first, second, and third ~~conductive~~ means for selectively coupling the first or second means to the third means for electrical connection,

wherein the first and second means are external to the integrated circuit.

19. (Original) The apparatus of claim 18, further comprising a circuit board supporting the first multiplexer and the first, second, and third means.

20. (Original) The apparatus of claim 18, wherein the third means is for connection to one of a test clock node, a test-data-input node, a test-mode-select node, and a test-data-out node of the test-access port.

21. (Currently Amended) The apparatus of claim 18, further comprising:

fourth means for connection to a node of the tester ~~first TAP control device~~;

fifth means for connection to a node of the ~~second~~ TAP master controller ~~control device~~;

sixth means for connection to a node of the test-access-port; and

a second multiplexer coupled to the fourth, fifth, and sixth ~~conductive~~ means for selectively coupling the fourth or fifth conductive means to the sixth conductive means.

22. (Currently Amended) Apparatus comprising:

a first connector for connection to an automatic tester ~~a first TAP control device~~;

a second connector for connection to a ~~second~~ TAP master controller ~~control device~~;

a third connector for connection to a test-access-port of an integrated circuit; and

a first multiplexer coupled to respective first, second, and third nodes of the first, second, and third connectors for selectively coupling the first or second nodes to the third nodes, wherein the first multiplexer includes a control input coupled to the automatic tester, the first multiplexer operable to selectively couple the first connect to the third connector or the second connector to the third connector

based on whether the tester is asserting a control signal on the control input, and wherein the first TAP master controller ~~control device~~ and the first multiplexer are external to the integrated circuit.

23. (Original) The apparatus of claim 22, further comprising a circuit board supporting the first multiplexer and the first, second, and third connectors.

24. (Original) The apparatus of claim 22, wherein each of the first, second, and third connectors includes a test clock node, a test-data-input node, a test-mode-select node, and a test-data-out node.

25. (Currently Amended) A machine-readable medium comprising:

coded instructions for operating a switching device to selectively couple one of a tester and a TAP master controller ~~plurality of TAP controllers~~ to a TAP in an integrated circuit,

further including coded instructions for operating the tester ~~a device~~ to detect a condition of the integrated circuit while ~~using a first TAP controller~~ the tester is selectively coupled to the TAP and in response to the detection of the condition, selectively coupling the TAP master controller to the TAP for communicating with the TAP using ~~a second~~ the TAP master controller ~~control device~~ in response to detection of the condition.

26. (Canceled)

27. (Original) The medium of claim 25, wherein the condition is a failure of the integrated circuit.

28. (Original) The medium of claim 25, wherein the medium comprises an electronic, optical, or magnetic memory.

29-30. (Canceled)